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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,148	06/29/2000	Takehiko Tsuchiya	03180.0255	7735
22852	7590	06/01/2005	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			CHANG, SUNRAY	
			ART UNIT	PAPER NUMBER
			2121	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/606,148

Applicant(s)

TSUCHIYA ET AL.

Examiner

Sunray Chang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in responsive to the paper 6 filed on April 5th, 2004
2. Claims 1 – 16 are presented for examination.

Claims 1 – 16 are rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Gilbert et al. (U.S. Patent No. 5,805,861, and referred to as **Gilbert** hereinafter).
4. Regarding independent claims 1, 3, and 8, **Gilbert** teaches,
 - A logic verification unit configured to perform a logic verification [CGC, Fig. 6] by inputting a plurality of test vectors [user-defined names, Col. 11, Lines 55 – 61] necessary for the logic verification [Cone Graph Compare processing, Col. 11, Lines 62 – 67] to a circuit description defining a structure and a specification of a circuit to be designed [old design & new design, Col. 11, Line 62 – Col. 12, Line 3] and comparing an output signal and an expected value of the output signal [new logic is different than the old logic], and judging the validity of the

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circuit description [to omit or commit the updated (new) design, Col. 12, Lines 13 – 14]; [see also Col. 11, Line 55 – Col. 12, Line 37, and Fig. 6 & 7]

- A profile information generating unit configured to store information [database, 42 – 44, Fig. 4] about a plurality of logic cones [cone of logic, 48, Fig. 4] in the circuit description [design version, 48, Fig. 4] to be activated by the test vectors during the logic verification in every test vector [comparing the old and new designs and assigning new names as needed, Col. 12, Lines 7 – 8] as a profile information [design version, 42 – 46, Fig. 4];
- A circuit changing unit configured to change the circuit description [Col. 11, Lines 49 – 54] after the logic verification and to generate a changed circuit description [Col. 11, Lines 36 – 38];
- A logic cone specifying unit configured to specify changed logic cones of the changed circuit description based on a result of a formal verification [indicates the condition where the new logic is different than the old logic, Col. 12, Lines 11 – 12]; and
- A test vector classifying unit configured to classify [transfer, 54, 58, Fig. 4] the test vectors [new components and net names, Col. 12, Line 28] into test vectors ~~related to~~ activating the changed logic cones [new design, Col. 12, Line 25] and test vectors ~~unrelated to~~ not activating the changed logic cones by using the profile information [whether to omit or commit the updated (new) design ... the changes to the new design are accepted, Col. 12, Lines 35 – 37].
- Wherein the logic verification unit [CGC, Fig. 6] performs a logic verification [Cone Graph Compare processing, Col. 11, Lines 55 – 61] of the changed circuit description [new design,

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Col. 12, Line 25] using the test vectors related to activating the changed logic cones [the changes to the new design are accepted, Col. 12, Lines 35 – 37].

5. Regarding dependent claims 2, 4, and 11,

- A logic cone dividing unit [46, Fig. 4] configured to divide [46, Fig. 4] the circuit description [design version, 46, Fig. 4] into the logic cones [cones of logic, 46, Fig. 4];
- A formal verification unit for verifying [verified, Col 7, Line 9] by formal technology [desired specification, Col 7, Line 10] using first and second circuit descriptions [behavior, detailed description, Col 7, Line 10 – 12];

6. Regarding dependent claims 5, 9 and 12, Gilbert teaches,

- Logic verification [Cone Graph Compare processing, Col. 11, Lines 62 – 67] of the changed circuit description [corrected design, Col 12, Line 9] is executed [assigned, Col 12, Line 7] by using preferentially the test vectors [new components and net names, Col. 12, Line 28] ~~relating to~~ activating the changed logic cones [the changes to the new design are accepted, Col. 12, Lines 35 – 37].

7. Regarding dependent claims 6 and 10, Gilbert teaches,

- Issuing conversion process, Col 7, Line 13] a circuit description [detailed description, Col 7, Line 14] and processing [complete, Col 7, Line 20] circuit manufacture [layout, Col 7, Line 22] by using the circuit description [detailed description, Col 7, Line 18].

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8. Regarding dependent claim 7, Gilbert teaches,

- Issuing [conversion process, Col 7, Line 13] a circuit description [detailed description, Col 7, Line 14] and processing circuit design [remaining design processes, Col 7, Line 17] and manufacture [layout, Col 7, Line 22] by using the circuit description [detailed description, Col 7, Line 14].

9. Regarding dependent claims 13, 15 and 16,

- **Second and subsequent logic verifications** are executed by using **only the test vectors** relating to **activating** the **changed logic cones**.

Gilbert teaches incremental design changes [**changed logic cones**] do not result [**only**] in unnecessary modifications [**activating**] to placement and routing information because of name changes [**test vectors**]. Therefore, large amounts of time are saved in the design and test cycle [**second and subsequent logic verifications**] for integrated circuits because the result of previous design [unchanged parts] can be reused. [Col. 17, Line 33 – 39]

10. Regarding dependent claim 14,

- The **logic cone specifying unit** specifies the **changed logic cones** on the basis of a **result of the formal verification**.

Gilbert teaches **logic cone specifying unit** [48, Fig. 4] specifies the **changed logic cones** [cone of logic from new design, 48, Fig. 4].

Gilbert further teaches errors [**a result**] may be detected during the simulation and testing phases [**formal verification**] of the design cycle and then fixed [**changed**] in the behavioral description [**logic cones**]. [Col. 2, Line 38 – 40]

Response to Amendment

Claim Rejections - 35 USC § 102

11. Applicants' argument regarding examiner is making a prohibited piecemeal rejection that the term "test vectors" has been read on three different terms "design change flag", "select cone of logic from both design version" and "names".

The Examiner has withdrawn the forth rejection and new paragraphs in **Gilbert** have been cited for new rejections.

Assuming that applicants' assumption is correct, the two inventions are different, does not render the 35 USC §102 rejection to be in error. Under 35 USC §102, all that is required is for the reference to disclose the same limitation as applicant claims, and this, applicants agree with. Applicants argue features disclosed in the specification and not set forth in the claims. Features from the specification are not read into the claims and therefore, the rejection is maintained.

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Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sunray Chang whose telephone number is (571) 272-3682. The examiner can normally be reached on M-F 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (571) 272-3687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-746-3506.

Sunray Chang
Patent Examiner
Group Art Unit 2121
Technology Center 2100
U.S. Patent and Trademark Office



Anthony Knight
Supervisory Patent Examiner
Group 3600

May 16, 2005